AMENDMENTS TO THE CLAIMS

1. (**Cancelled**)

2. (**Cancelled**)

3. (**Currently Amended**) A Wave Dynamic Differential Logic, comprising:

a plurality of differential logic cells arranged in a combinatorial logic tree and each having inverted combinatorial data-bearing inputs and corresponding non-inverted combinatorial data-bearing inputs, each of said plurality of differential logic cells configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, each of said plurality of differential logic cells configured to receive a precharge wave and/or a predischarge wave on said inverted combinatorial data-bearing inputs and non-inverted combinatorial data-bearing inputs of the respective differential logic cell and to propagate said precharge wave and/or said predischarge wave from said inverted combinatorial data-bearing inputs and corresponding non-inverting combinatorial data-bearing inputs of the respective differential logic cell to said inverted logic outputs and said non-inverted logic outputs of the respective differential logic cell,

wherein each of said plurality of differential logic cells is configured to receive and propagate said precharge wave and/or said predischarge wave during a precharge and/or pre-discharge phase, and is further configured to, during an evaluation phase, receive differential data on its inverted inputs and its corresponding non-inverted inputs and evaluate said differential data to produce differential output data on its inverted logic outputs and its non-inverted logic outputs.

wherein said precharge wave and/or said predischarge wave is encoded in data received on the inverted and non-inverted combinatorial data-bearing inputs of each of said plurality of differential logic cells, and

wherein each of said plurality of differential logic cells is precharged or predischarged without distributing a separate precharge or predischarge signal to the plurality of differential logic cells.

4. (**Currently Amended**) A Wave Dynamic Differential Logic, comprising:

a plurality of differential logic cells each having inverted combinatorial data-bearing inputs and corresponding non-inverted combinatorial data-bearing inputs, each of said plurality of differential logic cells configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs; and

a pre-discharged logic cell configured to receive a pre-discharge signal and, in response to said pre-discharge signal, to generate a pre-discharge wave to pre-discharge and propagate through each of said plurality of differential logic cells from said inverted combinatorial data-bearing inputs and non-inverted combinatorial data-bearing inputs of the respective differential logic cell to said inverted logic outputs and non-inverted logic outputs of the respective differential logic cell and/or a precharged logic cell configured to receive a precharge signal and, in response to said precharge signal, to generate a precharge wave to pre-charge and propagate through each of said plurality of differential logic cells from said inverted combinatorial data-bearing inputs and non-inverted combinatorial data-bearing inputs of the respective differential logic cell to said inverted logic outputs and non-inverted logic outputs of the respective differential logic cell,

wherein said precharge wave and/or said predischarge wave is encoded in data received on the inverted and non-inverted combinatorial data-bearing inputs of each of the plurality of differential logic cells, and

wherein each of said plurality of differential logic cells is predischarged or precharged without distributing a separate predischarge or precharge signal to the plurality of differential logic cells.

5. (**Currently Amended**) A Wave Dynamic Differential Logic, comprising:

a plurality of differential logic cells arranged in a combinatorial logic tree and each having inverted combinatorial data-bearing inputs and corresponding non-inverted combinatorial data-bearing inputs, each of said plurality of differential logic cells configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs; and

a precharge operator comprising first and second outputs and configured to receive a precharge signal and differential data comprising inverted differential data and corresponding non-inverted differential data, the precharge operator configured, during an evaluation phase, to provide the inverted differential data on the first output and the non-inverted differential data on the second output, and, during a precharge phase, to provide the precharge signal on the first and second outputs;

a ~~master-slave~~ differential ~~dynamic~~ logic register comprising a first output and a second output and configured to:

during the precharge phase, to receive a precharge signal and, in response to said precharge signal, to generate a pre-charge wave and provide the pre-charge wave to the combinatorial logic tree on the first second outputs to pre-charge and propagate through each of said plurality of differential logic cells from said inverted inputs and non-inverted inputs of the respective differential logic cell to said inverted logic outputs and non-inverted logic outputs of the respective differential logic cell; and

during the evaluation phase, to provide the differential data to the combinatorial logic tree on the first and second outputs; and

wherein said precharge wave is encoded in data received on the inverted and non-inverted combinatorial data-bearing inputs of each of the plurality of differential logic cells and each of said plurality of differential logic cells is precharged without distributing a separate precharge signal to any of the plurality of differential logic cells.

6. (**Currently Amended**) A Wave Dynamic Differential Logic, comprising:

a plurality of differential logic cells arranged in a combinatorial logic tree and each having combinatorial data-bearing inverted inputs and corresponding non-inverted combinatorial data-bearing inputs, each of said plurality of differential logic cells configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs; and

a predischarge operator comprising first and second outputs, and configured to receive a predischarge signal and differential data comprising inverted differential data and corresponding non-inverted differential data, the predischarge operator configured, during an evaluation phase, to provide the inverted differential data on the first output and the non-inverted differential data on the second output, and, during a predischarge phase, to provide the predischarge signal on the first and second outputs;

a ~~master-slave~~ differential ~~dynamic~~ logic register comprising first a second outputs and configured to:

during the predischarge phase, to receive a pre-discharge signal and, in response to said pre-discharge signal, to generate a pre-discharge wave and provide the predischarge wave to the combinatorial logic tree on the first and second outputs ~~in response to said pre-discharge signal~~ to pre-discharge and propagate through each of said differential logic cells from said inverted inputs and non-inverted inputs of the respective differential logic cell to said inverted logic outputs and non-inverted logic outputs of the respective differential logic cell; and

during the evaluation phase, to provide the differential data to the combinatorial logic tree on the first and second outputs; and

wherein said predischarge wave is encoded in data received on the inverted and non-inverted combinatorial data-bearing inputs of each of the plurality of differential logic cells and each of said plurality of differential logic cells is predischarged without distributing a separate predischarge signal to the plurality of differential logic cells.

7. (**Currently Amended**) A Divided Wave Dynamic Differential Logic DPA-resistant logic circuit, comprising:

a first single-ended logic tree comprising a plurality of first combinatorial data-bearing logic tree inputs and a plurality of first logic tree outputs and configured to, during an evaluation phase, receive inverted input data and corresponding non-inverted input data on said first combinatorial data-bearing logic tree inputs and to produce first output data on said first logic tree outputs, the first logic tree comprising a first plurality of logic gates; and

a single-ended dual of said first single-ended logic tree connected in parallel with the first single-ended logic tree and comprising a plurality of dual combinatorial data-bearing logic tree inputs and a plurality of dual logic tree outputs and configured to, during said evaluation phase, receive said inverted input data and said corresponding non-inverted input data on said dual combinatorial data-bearing logic tree inputs and produce inverted first output data on said dual logic tree outputs, the dual of said first logic tree comprising a second plurality of logic gates, the first output data comprising single-ended non-inverted output data and the second output data comprising single-ended corresponding inverted output data,

said first logic tree and said dual of said first logic tree further configured to, during a precharge and/or pre-discharge phase, receive a precharge wave and/or a pre-discharge wave on said first combinatorial data-bearing logic tree inputs and said dual combinatorial data-bearing logic tree inputs and propagate said precharge wave and/or pre-discharge wave through each of the first

plurality of logic gates and each of the second plurality of logic gates to said first logic tree outputs and said dual logic tree outputs,

wherein said precharge wave is encoded in data received on the combinatorial data-bearing logic tree inputs of the first logic tree and the dual combinatorial data-bearing logic tree inputs of the second logic tree, and

wherein each of said first plurality of logic gates and each of said second plurality of logic gates is precharged or pre-discharged without distributing a separate precharge or pre-discharge signal to the first plurality of logic gates or to the second plurality of differential logic gates.

8. (**Cancelled**)

9. (**Currently Amended**) A Wave Dynamic Differential Logic, comprising:

a plurality of differential logic cells each having inverted combinatorial data-bearing inputs and corresponding non-inverted combinatorial data-bearing inputs, each of said differential logic cells configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs; and

a master-slave differential dynamic logic register configured to receive a pre-charge wave and to ~~transmits~~ transmit on the pre-charge wave to pre-charge each of said plurality of differential logic cells, each of the plurality of differential logic cells further configured to receive the precharge wave on said inverted combinatorial data-bearing inputs and non-inverted combinatorial data-bearing inputs of the respective differential logic cell and to propagate said pre-charge wave from said inverted combinatorial data-bearing inputs and corresponding non-inverting combinatorial data-bearing inputs of the respective differential logic cell to said inverted logic outputs and said non-inverted logic outputs of the respective differential logic cell,

wherein said precharge wave is encoded in data received on the inverted and non-inverted combinatorial data-bearing inputs of each of the plurality of differential logic cells, and

wherein each of said plurality of differential logic cells is pre-charged without distributing a separate pre-charge signal to the plurality of differential logic cells.

10. (**Currently Amended**) A Wave Dynamic Differential Logic, comprising:

a plurality of differential logic cells each having inverted combinatorial data-bearing inputs and corresponding non-inverted combinatorial data-bearing inputs, each of said plurality of differential logic cells configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs; and

a differential dynamic logic register configured to receive a pre-charge signal and, in response to said pre-charge signal, to generate a pre-charge wave to pre-charge each of said plurality of differential logic cells, each of said plurality of the differential logic cells further configured to receive the precharge wave on said inverted combinatorial data-bearing inputs and non-inverted combinatorial data-bearing inputs of the respective differential logic cell and to propagate said pre-charge wave from said inverted combinatorial data-bearing inputs and corresponding non-inverting combinatorial data-bearing inputs of the respective differential logic cell to said inverted logic outputs and said non-inverted logic outputs of the respective differential logic cell,

wherein said precharge wave is encoded in data received on the inverted and non-inverted combinatorial data-bearing inputs of each of the plurality of differential logic cells, and

wherein each of said plurality of differential logic cells is pre-charged without distributing a separate pre-charge signal to the plurality of differential logic cells.

11. (**Currently Amended**) A Wave Dynamic Differential Logic, comprising:

a plurality of differential logic cells each having inverted combinatorial data-bearing inputs and corresponding non-inverted combinatorial data-bearing inputs, each of said differential logic cell configured to provide one or more inverted combinatorial data-bearing logic outputs and corresponding one or more non-inverted combinatorial data-bearing logic outputs; and

a master-slave differential dynamic logic register configured to receive a pre-discharge wave and to ~~transmits~~ transmit on the pre-discharge wave to pre-discharge each of said plurality of differential logic cells, each of the plurality of differential logic cells further configured to receive the pre-discharge wave on said inverted combinatorial data-bearing inputs and non-inverted combinatorial data-bearing inputs of the respective differential logic cell and to propagate said pre-discharge wave from said inverted combinatorial data-bearing inputs and corresponding non-inverting combinatorial data-bearing inputs of the respective differential logic cell to said inverted logic outputs and said non-inverted logic outputs of the respective differential logic cell,

wherein said pre-discharge wave is encoded in data received on the inverted and non-inverted combinatorial data-bearing inputs of each of the plurality of differential logic cells, and

wherein each of said plurality of differential logic cells is pre-discharged without distributing a separate pre-discharge signal to the plurality of differential logic cells.

12. (**Currently Amended**) A Wave Dynamic Differential Logic, comprising:

a plurality of differential logic cells each having inverted combinatorial data-bearing inputs and corresponding non-inverted combinatorial data-bearing inputs, each of said differential logic cell configured to provide one or more

inverted logic outputs and corresponding one or more non-inverted logic outputs; and

a differential dynamic logic register configured to receive a pre-discharge signal and generate a pre-discharge wave to pre-discharge each of said plurality of differential logic cells, each of the plurality of differential logic cells further configured to receive the pre-discharge wave on said inverted combinatorial data-bearing inputs and non-inverted combinatorial data-bearing inputs of the respective differential logic cell and to propagate said pre-discharge wave from said inverted combinatorial data-bearing inputs and corresponding non-inverting combinatorial data-bearing inputs of the respective differential logic cell to said inverted logic outputs and said non-inverted logic outputs of the respective differential logic cell,

wherein said pre-discharge wave is encoded in data received on the inverted and non-inverted combinatorial data-bearing inputs of each of the plurality of differential logic cells, and

wherein each of said plurality of differential logic cells is pre-discharged without distributing a separate pre-discharge signal to the plurality of differential logic cells.

13-22. (**Cancelled**)

23. (**Original**) The Wave Dynamic Differential Logic of Claim 3, comprising positive logic.

24. (**Original**) The Wave Dynamic Differential Logic of Claim 4, comprising positive logic.

25. (**Original**) The Wave Dynamic Differential Logic of Claim 5, comprising positive logic.

26. (**Original**) The Wave Dynamic Differential Logic of Claim 6, comprising positive logic.

27. (**Cancelled**)

28. (**New**) The Wave Dynamic Differential Logic of Claim 3, wherein the combinatorial logic tree has a relatively constant power consumption that does not depend on the content of the differential data.

29. (**New**) The Wave Dynamic Differential Logic of Claim 28, wherein the combinatorial logic tree forms part of a DPA-resistant encryption module.

30. (**New**) The Wave Dynamic Differential Logic of Claim 5, wherein the Wave Dynamic Differential Logic has a relatively constant power consumption that does not depend on the differential data.

31. (**New**) The Wave Dynamic Differential Logic of Claim 30, wherein the Wave Dynamic Differential Logic forms part of a DPA-resistant encryption module.

32. (**New**) The Wave Dynamic Differential Logic of Claim 6, wherein the Wave Dynamic Differential Logic has a relatively constant power consumption that does not depend on the differential data.

33. (**New**) The Wave Dynamic Differential Logic of Claim 32, wherein the Wave Dynamic Differential Logic forms part of a DPA-resistant encryption module.

34. (**New**) The Wave Dynamic Differential Logic of Claim 7, wherein the logic circuit has a relatively constant power consumption that does not depend on the differential data.

35. (**New**) The Wave Dynamic Differential Logic of Claim 7, wherein the single-ended dual is derived from the first single-ended logic tree.

36. (**New**) The Wave Dynamic Differential Logic of Claim 35, wherein the first plurality of logic gates of the first single-ended logic tree comprise one or more AND gates and one or more OR gates, and wherein the second plurality of logic gates of the single-ended dual comprise:

one or more OR gates corresponding to each of the one or more AND gates of the first plurality of logic gates; and

one or more AND gates corresponding to each of the one or more OR gates of the first plurality of logic gates.